AMENDMENTS TO THE SPECIFICATION

Please replace the first paragraph on page 6 with the following amended paragraph:

In Fig. 2, which is a block circuit diagram of a first driving apparatus for driving the LCD units 104 and 105 of Figs. 1A , 1B, 1C and 1D, the main LCD unit 104 is of a high quality thin film transistor (TFT)-type having 144×176 pixels which is expensive, and the sub LCD unit 105 is a low quality super twisted nematic (STN)-type LCD unit having 64×96 pixels which is inexpensive. The main LCD unit 101 is driven by a data driver circuit 201 and a scan driver circuit 202, while the sub LCD unit 102 is driver by a column driver circuit 203 and a row driver circuit 204. The data driver circuit 201, the scan driver circuit 202, the column driver circuit 203 and the row driver circuit 204 are controlled by a display control circuit 205 which is also controlled by a central processing unit (CPU) 206. The display control circuit 205 controls a power supply control circuit 207 which supplies power supply voltages to a common electrode CE1 of the main LCD unit 101, a common electrode CE2 of the sub LCD unit 102, the data driver circuit 201, the scan driver circuit 202, the column driver circuit 203 and the row driver circuit 204.

Please replace the fourth paragraph bridging pages 6-7 with the following amended paragraph:

In Fig. 3, which is a block circuit diagram of a second driving apparatus for driving the LCD units 105 and 107 of Figs. 1A, 1B, 1C and 1D, the main LCD unit 104 and the sub LCD unit 105 are both of a TFT-type. In this case, the scan lines of the sub LCD unit 105 are short-circuited to the corresponding scan lines of the main LCD unit 104, so that the scan driver circuit 204 of Fig. 2 is omitted. Note that, if the data lines of the sub LCD unit 105 are short-circuited to

the corresponding data lines of the main LCD unit 104, the data driver circuit 203 of Fig. 2 can be omitted.

Please replace the first paragraph on page 11 with the following amended paragraph:

In Fig. 8, four voltage dividers 3071, 3072, 3073 and 3074 each having a series of resistors are provided. In this case, the voltage dividers 3071 and 3072 are used for a positive polarity operation (POL = "0"), while the voltage dividers 3073 and 3074 are used for a negative operation (POL = "1"). Also, the voltage dividers 3071 and 3073 are used for displaying the main LCD unit 1 (MC = "0"), while the voltage dividers 3072 and 3074 are used for displaying the sub LCD unit 2 (MC = "1"). Note that a control signal MC is in synchronization with the control signal MS and is delayed by one pulse of a vertical clock signal VCLK.

Please replace the second paragraph on page 14 with the following amended paragraph:

Also, in the selection circuit ~~309~~405, when the control signal MC is "0"(low), the switches SW3A are turned ON and the switches SW3B are turned OFF, so that the main LCD unit 1 is operated. On the other hand, when the control signal MC is "1"(high), the switches SW3A are turned OFF and the switches SW3B are turned ON, so that the sub LCD unit 2 is operated.

Please replace the first paragraph on page 15 with the following amended paragraph:

The operation of the data driver circuit 3 and the scan driver circuit 4 of Fig. ~~14~~ 4 is explained next with reference to Figs. 15, 16, 17, 18 and 19.